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(54) Interleave read address generator

(57) An interleaver for use in a CDMA mobile station is arranged into a matrix of 32 rows and 18 columns. Interleave data is written to the interleave memory in column order and, within each column, in row order. A base-18 counter counts a clock input modulo-18, to generate a column address c5-c9, and a base-32 counter counts carry outputs from the base-18 counter modulo-32, to generate a row count value. A multiplexer MUX changes the positions of the bits of the row count value according to one or more data rate selection signals S0-S3, to generate a row address c0-c4. The interleave data is read from the interleave memory at the position corresponding to the column and row addresses.

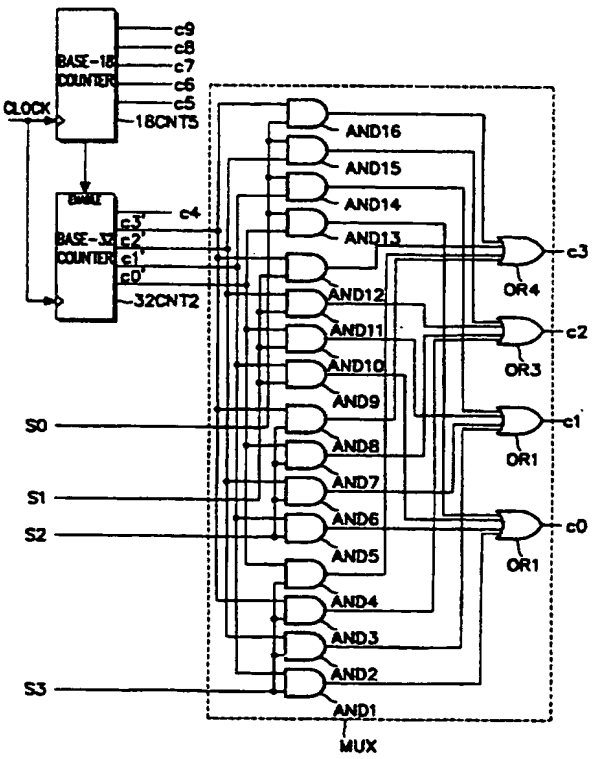

FIG. 11

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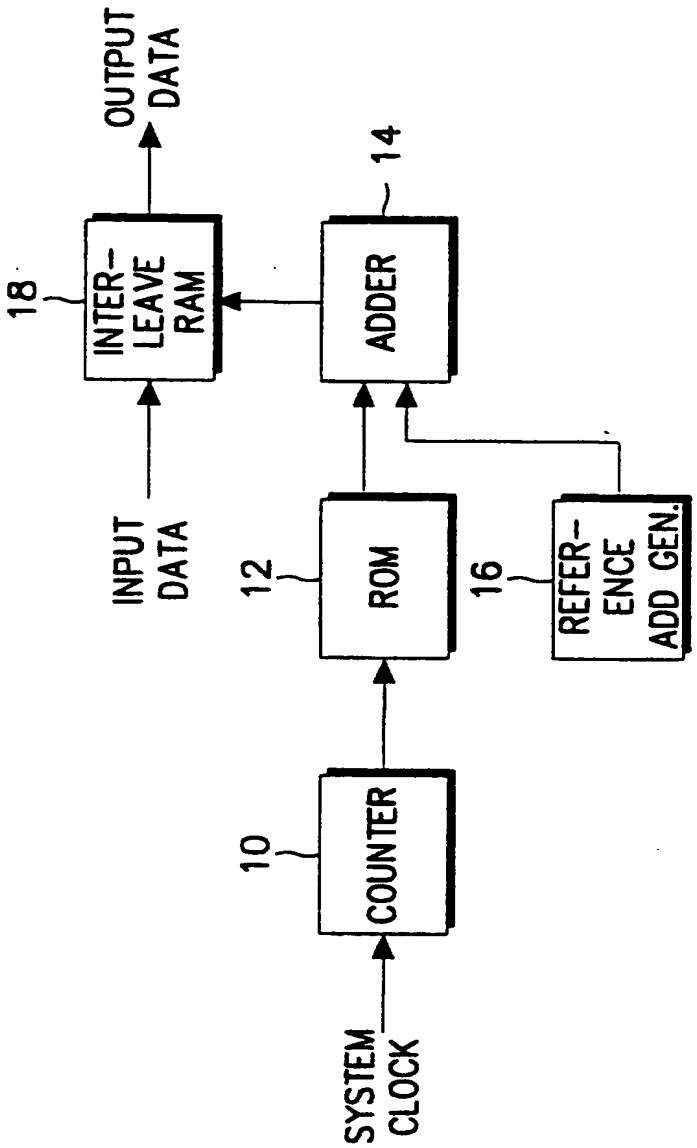

FIG. 1

1	33	65	97	129	161	193	225	257	289	321	353	385	417	449	481	513	545
2	34	66	98	130	162	194	226	258	290	322	354	386	418	450	482	514	546
3	35	67	99	131	163	195	227	259	291	323	355	387	419	451	483	515	547
4	36	68	100	132	164	196	228	260	292	324	356	388	420	452	484	516	548
5	37	69	101	133	165	197	229	261	293	325	357	389	421	453	485	517	549
6	38	70	102	134	166	198	230	262	294	326	358	390	422	454	486	518	550
7	39	71	103	135	167	199	231	263	295	327	359	391	423	455	487	519	551
8	40	72	104	136	168	200	232	264	296	328	360	392	424	456	488	520	552
9	41	73	105	137	169	201	233	265	297	329	361	393	425	457	489	521	553
10	42	74	106	138	170	202	234	266	298	330	362	394	426	458	490	522	554
11	43	75	107	139	171	203	235	267	299	331	363	395	427	459	491	523	555
12	44	76	108	140	172	204	236	268	300	332	364	396	428	460	492	524	556
13	45	77	109	141	173	205	237	269	301	333	365	397	429	461	493	525	557
14	46	78	110	142	174	206	238	270	302	334	366	398	430	462	494	526	558
15	47	79	111	143	175	207	239	271	303	335	367	399	431	463	495	527	559
16	48	80	112	144	176	208	240	272	304	336	368	400	432	464	496	528	560
17	49	81	113	145	177	209	241	273	305	337	369	401	433	465	497	529	561
18	50	82	114	146	178	210	242	274	306	338	370	402	434	466	498	530	562
19	51	83	115	147	179	211	243	275	307	339	371	403	435	467	499	531	563
20	52	84	116	148	180	212	244	276	308	340	372	404	436	468	500	532	564
21	53	85	117	149	181	213	245	277	309	341	373	405	437	469	501	533	565
22	54	86	118	150	182	214	246	278	310	342	374	406	438	470	502	534	566
23	55	87	119	151	183	215	247	279	311	343	375	407	439	471	503	535	567
24	56	88	120	152	184	216	248	280	312	344	376	408	440	472	504	536	568
25	57	89	121	153	185	217	249	281	313	345	377	409	441	473	505	537	569
26	58	90	122	154	186	218	250	282	314	346	378	410	442	474	506	538	570
27	59	91	123	155	187	219	251	283	315	347	379	411	443	475	507	539	571
28	60	92	124	156	188	220	252	284	316	348	380	412	444	476	508	540	572
29	61	93	125	157	189	221	253	285	317	349	381	413	445	477	509	541	573
30	62	94	126	158	190	222	254	286	318	350	382	414	446	478	510	542	574
31	63	95	127	159	191	223	255	287	319	351	383	415	447	479	511	543	575
32	64	96	128	160	192	224	256	288	320	352	384	416	448	480	512	544	576

FIG. 2

1	17	33	49	65	81	97	113	129	145	161	177	193	209	225	241	257	273
1	17	33	49	65	81	97	113	129	145	161	177	193	209	225	241	257	273
2	18	34	50	66	82	98	114	130	146	162	178	194	210	226	242	258	274
2	18	34	50	66	82	98	114	130	146	162	178	194	210	226	242	258	274
3	19	35	51	67	83	99	115	131	147	163	179	195	211	227	243	259	275
3	19	35	51	67	83	99	115	131	147	163	179	195	211	227	243	259	275
4	20	36	52	68	84	100	116	132	148	164	180	196	212	228	244	260	276
4	20	36	52	68	84	100	116	132	148	164	180	196	212	228	244	260	276
5	21	37	53	69	85	101	117	133	149	165	181	197	213	229	245	261	277
5	21	37	53	69	85	101	117	133	149	165	181	197	213	229	245	261	277
6	22	38	54	70	86	102	118	134	150	166	182	198	214	230	246	262	278
6	22	38	54	70	86	102	118	134	150	166	182	198	214	230	246	262	278
7	23	39	55	71	87	103	119	135	151	167	183	199	215	231	247	263	279
7	23	39	55	71	87	103	119	135	151	167	183	199	215	231	247	263	279
8	24	40	56	72	88	104	120	136	152	168	184	200	216	232	248	264	280
8	24	40	56	72	88	104	120	136	152	168	184	200	216	232	248	264	280
9	25	41	57	73	89	105	121	137	153	169	185	201	217	233	249	265	281
9	25	41	57	73	89	105	121	137	153	169	185	201	217	233	249	265	281
10	26	42	58	74	90	106	122	138	154	170	186	202	218	234	250	266	282
10	26	42	58	74	90	106	122	138	154	170	186	202	218	234	250	266	282
11	27	43	59	75	91	107	123	139	155	171	187	203	219	235	251	267	283
11	27	43	59	75	91	107	123	139	155	171	187	203	219	235	251	267	283
12	28	44	60	76	92	108	124	140	156	172	188	204	220	236	252	268	284
12	28	44	60	76	92	108	124	140	156	172	188	204	220	236	252	268	284
13	29	45	61	77	93	109	125	141	157	173	189	205	221	237	253	269	285
13	29	45	61	77	93	109	125	141	157	173	189	205	221	237	253	269	285
14	30	46	62	78	94	110	126	142	158	174	190	206	222	238	254	270	286
14	30	46	62	78	94	110	126	142	158	174	190	206	222	238	254	270	286
15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255	271	287
15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255	271	287
16	32	48	64	80	96	112	128	144	160	176	192	208	224	240	256	272	288
16	32	48	64	80	96	112	128	144	160	176	192	208	224	240	256	272	288

FIG. 3

1	9	17	25	33	41	49	57	65	73	81	89	97	105	113	121	129	137
1	9	17	25	33	41	49	57	65	73	81	89	97	105	113	121	129	137
1	9	17	25	33	41	49	57	65	73	81	89	97	105	113	121	129	137
1	9	17	25	33	41	49	57	65	73	81	89	97	105	113	121	129	137
2	10	18	26	34	42	50	58	66	74	82	90	98	106	114	122	130	138
2	10	18	26	34	42	50	58	66	74	82	90	98	106	114	122	130	138
2	10	18	26	34	42	50	58	66	74	82	90	98	106	114	122	130	138
2	10	18	26	34	42	50	58	66	74	82	90	98	106	114	122	130	138
3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139
3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139
3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139
3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139
4	12	20	28	36	44	52	60	68	76	84	92	100	108	116	124	132	140
4	12	20	28	36	44	52	60	68	76	84	92	100	108	116	124	132	140
4	12	20	28	36	44	52	60	68	76	84	92	100	108	116	124	132	140
4	12	20	28	36	44	52	60	68	76	84	92	100	108	116	124	132	140
5	13	21	29	37	45	53	61	69	77	85	93	101	109	117	125	133	141
5	13	21	29	37	45	53	61	69	77	85	93	101	109	117	125	133	141
5	13	21	29	37	45	53	61	69	77	85	93	101	109	117	125	133	141
5	13	21	29	37	45	53	61	69	77	85	93	101	109	117	125	133	141
6	14	22	30	38	46	54	62	70	78	86	94	102	110	118	126	134	142
6	14	22	30	38	46	54	62	70	78	86	94	102	110	118	126	134	142
6	14	22	30	38	46	54	62	70	78	86	94	102	110	118	126	134	142
6	14	22	30	38	46	54	62	70	78	86	94	102	110	118	126	134	142
7	15	23	31	39	47	55	63	71	79	87	95	103	111	119	127	135	143
7	15	23	31	39	47	55	63	71	79	87	95	103	111	119	127	135	143
7	15	23	31	39	47	55	63	71	79	87	95	103	111	119	127	135	143
7	15	23	31	39	47	55	63	71	79	87	95	103	111	119	127	135	143
8	16	24	32	40	48	56	64	72	80	88	96	104	112	120	128	136	144
8	16	24	32	40	48	56	64	72	80	88	96	104	112	120	128	136	144
8	16	24	32	40	48	56	64	72	80	88	96	104	112	120	128	136	144
8	16	24	32	40	48	56	64	72	80	88	96	104	112	120	128	136	144

FIG. 4

1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70
2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70
2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70
2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70
2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70
2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70
2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70
2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70
3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71
3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71
3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71
3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71
3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71
3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71
3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71
3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71
4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72
4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72
4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72
4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72
4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72
4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72
4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72
4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72

FIG. 5

DATA RATE	READING SEQUENCE OF ROW
9600 & 14400bps	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
4800 & 7200bps	1 3 2 4 5 7 6 8 9 11 10 12 13 15 14 16 17 19 18 20 21 23 22 24 25 27 26 28 29 31 30 32
2400 & 3600bps	1 5 2 6 3 7 4 8 9 13 10 14 11 15 12 16 17 21 18 22 19 23 20 24 25 29 26 30 27 31 28 32
1200 & 1800bps	1 9 2 10 3 11 4 12 5 13 6 14 7 15 8 16 17 25 18 26 19 27 20 28 21 29 22 30 23 31 24 32

FIG. 6

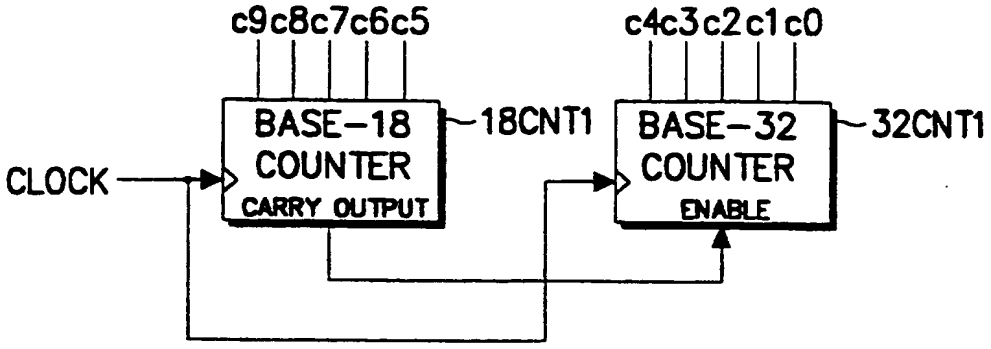

FIG. 7

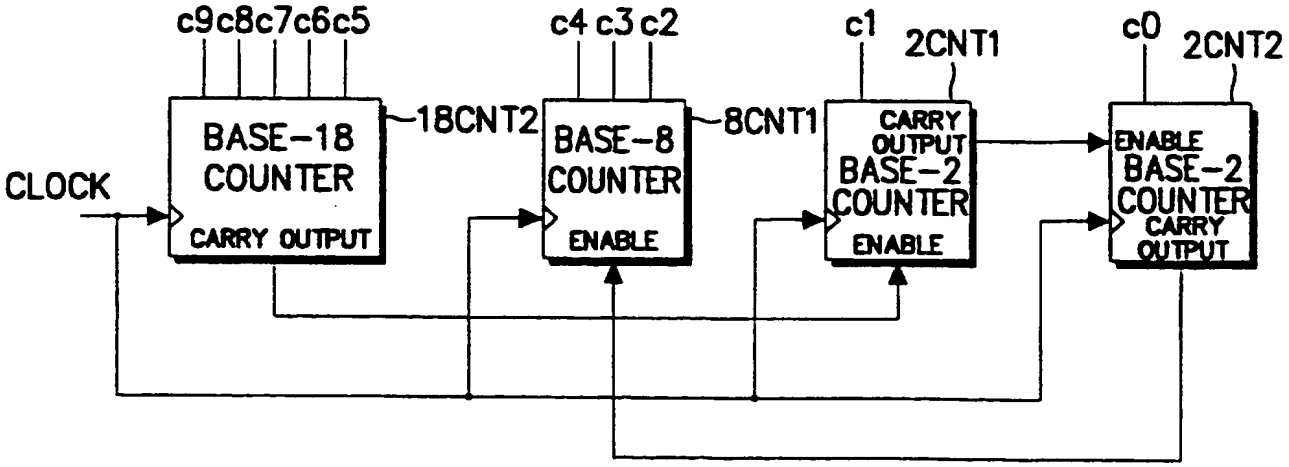

FIG. 8

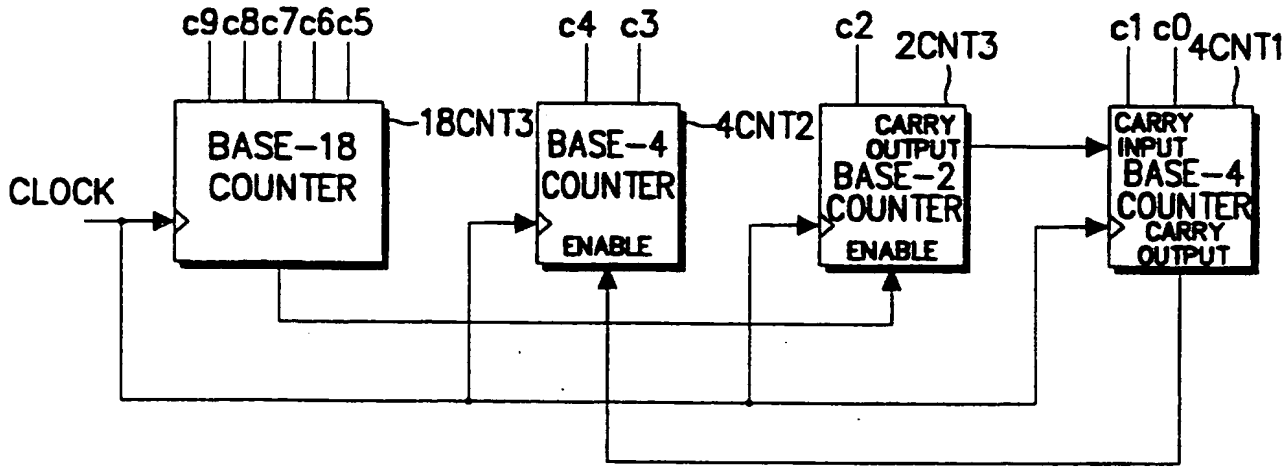

FIG. 9

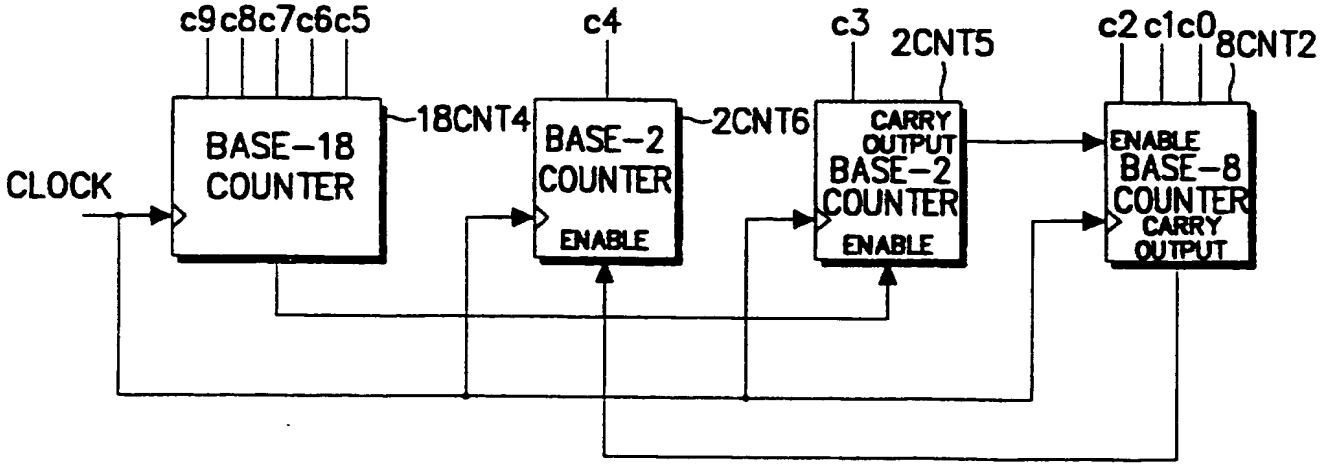

FIG. 10

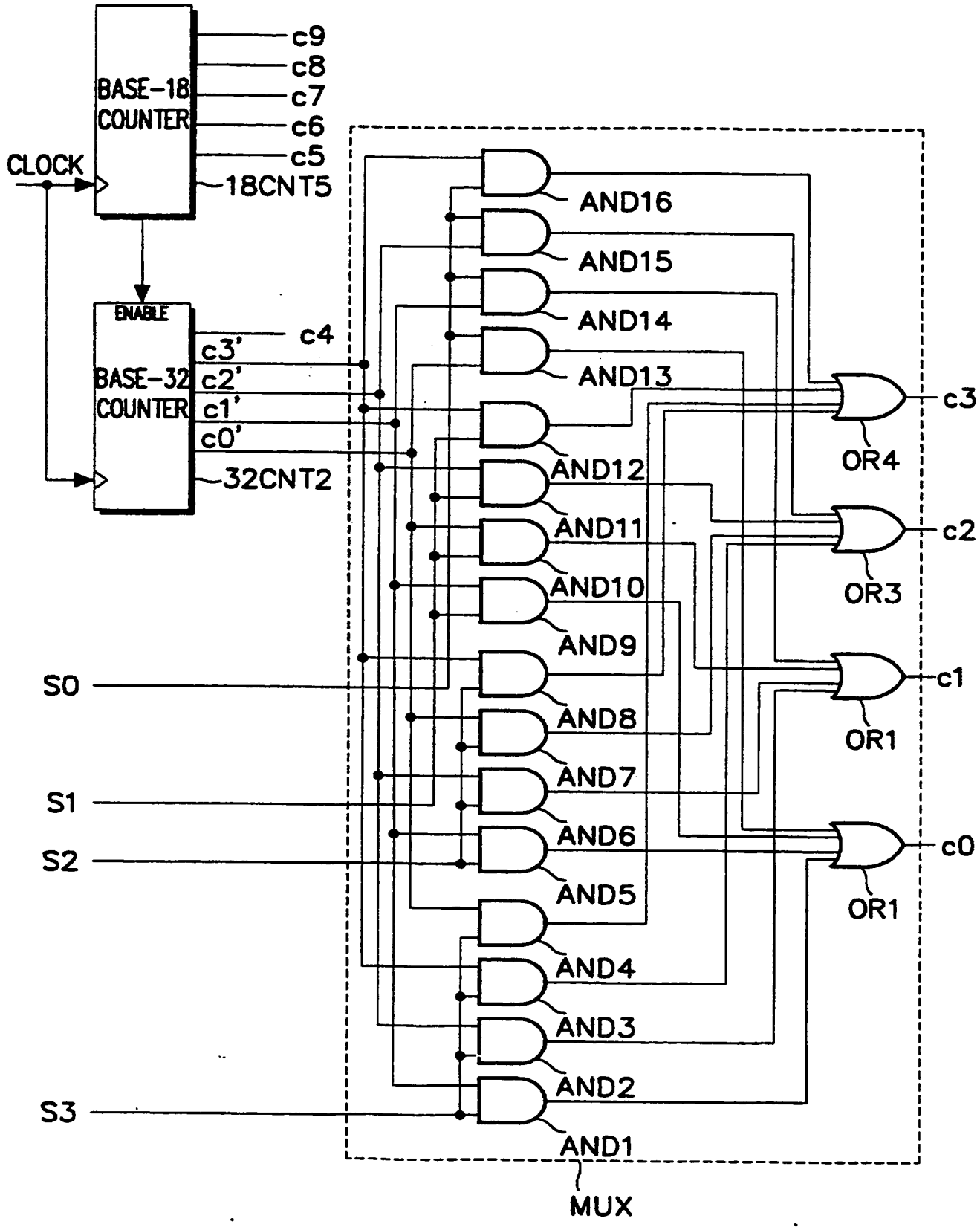

FIG. 11

INTERLEAVE READ ADDRESS GENERATOR

Background of the Invention

The present invention relates to an interleaver for use in a CDMA (Code Division Multiple Access) PCS (Personal Communications Services) mobile station and in particular to the structure of an interleave read address generator for generating an interleave read address for reading out data written in an interleave memory.

In accordance with Standard SP-3384 for a CDMA PCS mobile station, it is specified that a CDMA PCS mobile station should perform interleaving to prevent reverse channel burst errors. The interleaving is achieved by successively writing transmission data into an interleave memory and then successively reading out the data from the interleave memory.

Referring to Fig. 1, a conventional interleaver for achieving interleaving includes a counter 10, a ROM (Read Only Memory) 12, an adder 14, a reference address generator 16 and an interleave RAM (Random Access Memory) 18. The counter 10 counts a system clock and applies the count value to the ROM 12 into which an interleave read address corresponding to the count value is written. Upon receiving the count value, the ROM 12 generates the interleave read address corresponding to the count value. The reference address generator 16 generates a reference address for reading and writing data from/into the interleave RAM 18. The adder 14 adds the interleave read address output from the ROM 12 to the reference address output from the reference address generator 16, to generate the interleave read address with which the interleave RAM 18 reads out the data written in it. The interleave RAM 18 writes data input from the exterior, and reads out the data written in it according to the interleave read address output from the adder 14.

As can be appreciated from the foregoing descriptions, the conventional interleaver necessarily includes the expensive ROM into which the interleave read address is written, thus increasing the cost of manufacturing the interleaver.

In the meantime, in accordance with the above stated Standard SP-3384, the interleaver has a variable data rate. In other words, Standard SP-3384 specifies a data rate of 9600bps and 14400bps, a data rate of 4800bps and 7200bps, a data rate of 2400bps and 3600bps, and a data rate of 1200bps and 1800bps. The interleaver should perform the interleaving differently with respect to the respective data rates. Accordingly, a CDMA system with a variable data rate needs to include a ROM into which the interleave read addresses are written for all the data rates. If the data rate is variable as stated above, the ROM must include an increased amount of data, so that the ROM must increase in capacity and hence in price.

Summary of the Invention

It is therefore an object of the present invention to provide an interleaver using a simple interleave read address generator.

Accordingly, the present invention provides an interleaver for use in a CDMA mobile station comprising:

an interleave memory arranged into a matrix of 2^n rows and m columns (where m and n are integers);

means for writing interleave data to the interleave memory in column order and, within each column, in row order;

an interleave read address generator comprising a base-m counter for counting a clock input modulo-m, to generate a column address, and a base-2^n counter for counting carry outputs from the base-m counter modulo-2^n, to generate a row address; and

means for reading the interleave data from the interleave memory at the position corresponding to the column and row addresses from the interleave read address

generator.

For the Standard SP-3384 CDMA PCS, it is preferred that m be 18 and n be 5.

Preferably, in an interleaver for a data rate of 9600bps or 14400bps, the column address is equal to the current value of the base-m counter and the row address is equal to the current value of the base-2^n counter.

Preferably, in an interleaver for a data rate of 4800bps or 7200bps, the column address is equal to the current value of the base-m counter and the row address is equal to the current value of the base-2^n counter with the positions of the two least significant bits (LSB and LSB+1) being altered as follows:

LSB	->	LSB+1;
LSB+1	->	LSB.

Preferably, in an interleaver for a data rate of 2400bps or 3600bps, the column address is equal to the current value of the base-m counter and the row address is equal to the current value of the base-2^n counter with the positions of the three least significant bits (LSB, LSB+1 and LSB+2) being altered as follows:

LSB	->	LSB+2;
LSB+2	->	LSB+1;
LSB+1	->	LBS.

Preferably, in an interleaver for a data rate of 1200bps or 1800bps, the column address is equal to the current value of the base-m counter and the row address is equal to the current value of the base-2^n counter with the positions of the four least significant bits (LSB, LSB+1, LSB+2 and LSB+3) being altered as follows:

LSB	->	LSB+3;
LSB+3	->	LSB+2;
LSB+2	->	LSB+1;
LSB+1	->	LSB.

The present invention also provides an interleaver for use in a CDMA mobile station comprising:

an interleave memory arranged into a matrix of 2^n rows and m columns (where m and n are integers);

means for writing interleave data to the interleave memory in column order and, within each column, in row order;

an interleave read address generator comprising a base-m counter for counting a clock input modulo-m, to generate a column address, and a base-2^n counter for counting carry outputs from the base-m counter modulo-2^n, to generate a row count value and a multiplexer for changing the positions of the bits of the row count value according to one or more data rate selection signals, to generate a row address; and

means for reading the interleave data from the interleave memory at the position corresponding to the column and row addresses from the interleave read address generator.

Again, for the Standard SP-3384 CDMA PCS, it is preferred that m be 18 and n be 5.

Preferably, for a data rate of 9600bps or 14400bps, the multiplexer outputs the bits of the row count value unchanged in response to a first data rate selection signal.

Preferably, for a data rate of 4800bps or 7200bps, the multiplexer changes the positions of the two least significant bits (LSB and LSB+1) of the row count value as follows in response to a second data rate selection signal:

LSB -> LSB+1;
LSB+1 -> LSB.

Preferably, for a data rate of 2400bps or 3600bps, the multiplexer changes the positions of the three least significant bits (LSB, LSB+1 and LSB+2) of the row count value as follows in response to a third data rate selection

signal:

LSB	->	LSB+2;
LSB+2	->	LSB+1
LSB+1	->	LSB.

Preferably, for a data rate of 1200bps or 1800bps, the multiplexer changes the positions of the four least significant bits (LSB, LSB+1, LSB+2 and LSB+3) of the row count value as follows in response to a fourth data rate selection signal:

LSB	->	LSB+3;
LSB+3	->	LSB+2
LSB+2	->	LSB+1
LSB+1	->	LSB.

Brief Description of the Drawings

The present invention will now be described by way of example with reference to the accompanying drawings in which:

Fig. 1 is a block diagram of a conventional interleaver;

Fig. 2 shows the data arrangement when data is written into an interleave memory at data rate of 9600bps and 14400bps;

Fig. 3 shows the data arrangement when data is written into the interleave memory at a data rate of 4800bps and 7200bps;

Fig. 4 shows the data arrangement when data is written into the interleave memory at a data rate of 2400bps and 3600bps;

Fig. 5 shows the data arrangement when data is written into the interleave memory at a data rate of 1200bps and 1800bps;

Fig. 6 shows the reading sequence of rows for reading out data written into the interleave memory with respect to respective data rates;

Fig. 7 is a diagram of an interleave read address generator for generating an interleave read address for reading data at the data rate of 9600bps and 14400bps;

Fig. 8 is a diagram of an interleave read address generator for generating an interleave read address for reading data at the data rate of 4800bps and 7200bps;

Fig. 9 is a diagram of an interleave read address generator for generating an interleave read address for reading data at the data rate of 2400bps and 3600bps;

Fig. 10 is a diagram of an interleave read address generator for generating an interleave read address for reading data at the data rate of 1200bps and 1800bps; and

Fig. 11 is a diagram of a variable interleave read address generator for generating an interleave read address for reading data at a variable data rate.

Detailed Description of the Preferred Embodiment

Fig. 2 illustrates a data arrangement of an interleave memory such as a RAM, when data is written at a data rate of 9600bps and 14400bps in accordance with Standard SP-3384 for a CDMA PCS mobile station. In the drawing, since the number of data written is the same as the number of addresses, the numbers shown in Fig. 2 are the same as the addresses in the interleave memory. In other words, a number '1' represents first data and an address at a first row and the first column, a number '2' represents second data and an address at a second row and the first column. In the similar way, a number '3' represents third data and an address at a third row and the first column, etc. The other numbers represent the corresponding data and addresses, as described in the foregoing. It should be noted that such an address arrangement is also used for other data rates.

Referring to Fig. 2, the data are sequentially written in the order of the address at the data rate of 9600bps and 14400bps and the written data are read out according to the interleave read address during interleaving. Fig. 6 illustrates a reading sequence of the row addresses out of the interleave read addresses. As illustrated, the reading sequence of the rows at the data rate of 9600bps and 14400bps is 1, 2, 3, 4, ..., 32. Once the reading sequence

of the rows is determined, the data written in all eighteen columns of the determined rows are sequentially read out.

That is, with reference to Fig. 2, the reading sequence of the data at the data rate of 9600bps and 14400bps is 1, 33, 65, 97, 129, ..., 545, 2, 34, ..., and 576. Fig. 7 illustrates an interleave read address generator for generating the interleave read address in accordance with the above mentioned data reading sequence. The interleave read address generator includes a first base-18 (octadecimal) counter 18CNT1 and a first base-32 counter 32CNT1.

The interleave read addresses are represented by five column address bits c9, c8, c7, c6 and c5, and five row address bits c4, c3, c2, c1 and c0, respectively. As shown in Table 1, 32 rows are represented by the row address bits c4, c3, c2, c1 and c0. It should be noted that the rows can be represented in the same way by the row address bits c4, c3, c2, c1 and c0, at the other data rates.

<Table 1>

Rows	Bits					Rows	Bits				
	c4	c3	c2	c1	c0		c4	c3	c2	c1	c0
1	0	0	0	0	0	17	1	0	0	0	0
2	0	0	0	0	1	18	1	0	0	0	1
3	0	0	0	1	0	19	1	0	0	1	0
4	0	0	0	1	1	20	1	0	0	1	1
5	0	0	1	0	0	21	1	0	1	0	0
6	0	0	1	0	1	22	1	0	1	0	1
7	0	0	1	1	0	23	1	0	1	1	0
8	0	0	1	1	1	24	1	0	1	1	1
9	0	1	0	0	0	25	1	1	0	0	0

10	0	1	0	0	1	26	1	1	0	0	1
11	0	1	0	1	0	27	1	1	0	1	0
12	0	1	0	1	1	28	1	1	0	1	1
13	0	1	1	0	0	29	1	1	1	0	0
14	0	1	1	0	1	30	1	1	1	0	1
15	0	1	1	1	0	31	1	1	1	1	0
16	0	1	1	1	1	32	1	1	1	1	1

Further, as shown in Table 2, 18 columns are represented by the column address bits c9, c8, c7, c6, and c5. It should be noted that the columns are identically represented by the column address bits c9, c8, c7, c6 and c5, at the other data rates.

<Table 2>

Col	Bits					Col	Bits				
	c9	c8	c7	c6	c5		c9	c8	c7	c6	c5
1	0	0	0	0	0	10	0	1	0	0	1
2	0	0	0	0	1	11	0	1	0	1	0
3	0	0	0	1	0	12	0	1	0	1	1
4	0	0	0	1	1	13	0	1	1	0	0
5	0	0	1	0	0	14	0	1	1	0	1
6	0	0	1	0	1	15	0	1	1	1	0
7	0	0	1	1	0	16	0	1	1	1	1
8	0	0	1	1	1	17	1	0	0	0	0
9	0	1	0	0	0	18	1	0	0	0	1

That is, 576 addresses shown in Fig. 2 are represented by a combination of the column address bits c9, c8, c7, c6 and c5, and the row address bits c4, c3, c2, c1, and c0. For

example, an address at the first column and the first row is represented by a combination of the column address bits 00000 and the row address bits 00000.

Fig. 7 illustrates an interleave read address generator for generating the interleave read address in the sequence of the interleave read address for the data rate of 9600bps and 14400bps. In operation, the first base-18 counter 18CNT1 counts a clock input to generate a count value (i.e., the column address bits c9, c8, c7, c6 and c5, in which the column address bit c5 is the least significant bit (LSB) and the column address bit c9 is the most significant bit (MSB). Here, the count value represents the column address, and increases from 00000 corresponding to the first column to 10001 corresponding to the eighteenth column.

The first base-18 counter 18CNT1 generates a carry at a carry output terminal thereof when the count value changes from 10001 to 00000. The carry output from the first base-18 counter 18CNT1 is applied to an enable terminal of the first base-32 counter 32CNT1. Upon receiving the carry output from the first base-18 counter 18CNT1, the first base-32 counter 32CNT1 is enabled to count and to generate a count value of the row address bits c4, c3, c2, c1 and c0, in which the row address bit c0 is the least significant bit (LSB) and the row address bit c4 is the most significant bit (MSB). Here, the count value represents the row address, and sequentially increases from 00000 corresponding to the first row to 11111 corresponding to the thirty-second column.

As described above, the first base-18 counter 18CNT1 counts the clock from 00000 to 10001, to generate the column addresses 1, 33, 65, 129, 161, ..., and 545 shown in Fig. 2. The first base-18 counter 18CNT1 generates the carry when the count value changes from 10001 to 00000. Then, upon receiving the carry output from the first base-18 counter 18CNT1, the first base-32 counter 32CNT1 counts the

clock to generate a count value of 00001. At that moment, the first base-18 counter 18CNT1 again counts the clock from 00000 to 10001, to generate the column addresses 2, 34, 66, 98, 130, ..., and 546. In this manner, the interleave read address generator shown in Fig. 7 generates the interleave read addresses up to 576.

Fig. 3 illustrates a data arrangement when the data is written in the interleave memory at the data rate of 4800bps and 7200bps in accordance with Standard SP-3384 for the CDMA PCS mobile station. Although the addresses in the interleave memory are the same as those in case of 9600bps and 14400bps, the data rate of 4800bps and 7200bps is twice as low as the data rate of 9600bps and 14400bps. Accordingly, the data to be written into the interleave memory at the data rate of 4800bps and 7200bps are written at two sequential addresses. Therefore, the same data appears twice with respect to the whole data, as shown in Fig. 3. However, the data is interleaved by the address unit during the interleaving.

The data written sequentially into two addresses are read out according to the interleave read address, and the reading sequence of the rows of the interleave read addresses is illustrated in Fig. 6. Namely, Fig. 6 illustrates a sequence of the row addresses out of the interleave read addresses. As illustrated, the reading sequence of the rows at the data rate of 4800bps and 7200bps is 1, 3, 2, 4, 5, ..., and 32.

That is, the reading sequence at the data rate of 4800bps and 7200bps is 1, 33, 65, 129, ..., 545, 2, 34, ..., and 576. It is noted that the column sequence is the same as that in case of the data rate of 9600bps and 14400bps, but the row sequence is changed. The row address bits c4, c3, c2, c1 and c0 according to the reading sequence of the rows are represented by 00000, 00010, 00001, 00011, 00100, 00110, ... and 11111.

In general, a counter toggles the least significant bit (e.g., the bit c0) between 0 and 1, and toggles the next bit to least significant bit (i.e., the bit c1) when the least significant bit c0 is toggled from 1 to 0. However, at the data rate of 4800bps and 7200bps, the row address bit c1 is first toggled and then toggled in the sequence of the row address bits c0, c2, c3, and c4. Therefore, the interleave read address generator for the data rate of 4800bps and 7200bps can be realized by changing the output of the interleave read address generator for the data rate of 9600bps and 14400bps. Namely, the output bits c0 and c1 of the interleave read address generator for the data rate of 9600bps and 14400bps are exchanged with each other to realize the interleave read address generator for the data rate of 4800bps and 7200bps.

Fig. 8 illustrates the interleave read address generator for data rate of 4800bps and 7200bps. The interleave read address generator generates the interleave read address in the sequence of the interleave read address. The interleave read address generator includes a second base-18 counter 18CNT2, a first octal (base-8) counter 8CNT1, and first and second binary (base-2) counters 2CNT1 and 2CNT2. The second base-18 counter 18CNT2 generates the column address bits c9, c8, c7, c6 and c5 and a carry output in the same manner as the first base-18 counter 18CNT1 shown in Fig. 7, of the interleave read address generator for 9600bps and 14400bps. The carry output from the second base-18 counter 18CNT2 is applied to an enable terminal of the first binary counter 2CNT1 which receives the clock at a clock terminal thereof. Thus, whenever the carry output is received from the second base-18 counter 18CNT2, the first binary counter 2CNT1 counts the clock to generate the row address bit c1.

The first binary counter 2CNT1 generates a carry when the row address bit output c1 is changed from 1 to 0. The carry output from the first binary counter 2CNT1 is applied to an enable terminal of the second binary counter 2CNT2 which receives the clock at a clock terminal thereof. Thus, the

second binary counter 2CNT2 counts the clock to generate the row address bit c0, whenever the first binary counter 2CNT1 generates the carry.

The second binary counter 2CNT2 generates a carry whenever the row address bit output c0 changes from 1 to 0. The carry output from the second binary counter 2CNT2 is applied to an enable terminal of the first octal counter 8CNT1 which receives the clock at a clock terminal thereof. Thus, whenever the second binary counter 2CNT2 generates the carry output, the first octal counter 8CNT1 counts the clock to generate the row address bits c4, c3, and c2. Therefore, the interleave read address is generated in combination of the column address bits c9, c8, c7, c6 and c5 of the second base-18 counter 18CNT2, the row address bits c4, c3 and c2 of the octal counter 8CNT1, the row address bit c1 of the first binary counter 2CNT1, and the row address bit c0 of the second binary counter 2CNT2.

Fig. 4 illustrates a data arrangement when the data is written into the interleave memory at the data rate of 2400bps and 3600bps in accordance with Standard SP-3384 for the CDMA PCS mobile station. Although the addresses in the interleave memory are the same as those in case of 9600bps and 14400bps, the data rate of 2400bps and 3600bps is four times lower than the data rate of 9600bps and 14400bps. Accordingly, the data to be written into the interleave memory at the data rate of 2400bps and 3600bps are written at four sequential addresses. Therefore, the same data appears four times with respect to the whole data, as shown in Fig. 4. However, the data is interleaved by the address unit during the interleaving.

The data written sequentially into four addresses are read out according to the interleave read address during the interleaving, and the sequence of the rows of the interleave read addresses is illustrated in Fig. 6. Namely, Fig. 6 illustrates a sequence of the row addresses out of the interleave read addresses. As illustrated, the reading

sequence of the rows at the data rate of 2400bps and 3600bps is 1, 5, 2, 6, 3, 7, 4, 8, 9, 13, ..., and 32.

That is, the reading sequence at the data rate of 2400bps and 3600bps is to read 18 columns at the first row and then 18 columns at the fifth row, etc. It is noted that the column sequence is the same as that in case of the data rate of 9600bps and 14400bps, but the row sequence is changed. The row address bits c4, c3, c2, c1 and c0 according to the reading sequence of the rows are represented by 00000, 00100, 00001, 00101, 00010, 00110, ... and 11111.

It is noted from the foregoing descriptions that at the data rate of 2400bps and 3600bps, the row address bit c2 is first toggled and then toggled in the sequence of the bits c0, c1, c3, and c4. Therefore, the interleave read address generator for the data rate of 2400bps and 3600bps can be realized by changing the output of the interleave read address generator for the data rate of 9600bps and 14400bps. Namely, the output bits c0, c1 and c2 of the interleave read address generator for the data rate of 9600bps and 14400bps are changed respectively to the bits c2, c0 and c1 to realize the interleave read address generator for the data rate of 2400bps and 3600bps.

Fig. 9 illustrates the interleave read address generator for the data rate of 2400bps and 3600bps. The interleave read address generator generates the interleave read address in the sequence of the interleave read address. The interleave read address generator includes a third base-18 counter 18CNT3, first and second base-4 counters 4CNT1 and 4CNT2, and a third binary (base-2) counter 2CNT3. The third base-18 counter 18CNT3 generates the column address bits c9, c8, c7, c6 and c5 and a carry output in the same manner as the first base-18 counter 18CNT1 shown in Fig. 7, of the interleave read address generator for 9600bps and 14400bps. The carry output from the third base-18 counter 18CNT3 is applied to an enable terminal of the third binary counter

2CNT3 which receives the clock at a clock terminal thereof. Thus, whenever the third base-18 counter 18CNT3 generates the carry output, the third binary counter 2CNT3 counts the clock to generate the address bit c2.

The third binary counter 2CNT3 generates a carry when the address bit c2 is changed from 1 to 0. The carry output from the third binary counter 2CNT3 is applied to an enable terminal of the first base-4 counter 4CNT1 which receives the clock at a clock terminal thereof. Thus, the first base-4 counter 4CNT1 counts the clock to generate the address bits c1 and c0, whenever the third binary counter 2CNT3 generates the carry.

The first base-4 counter 4CNT1 generates a carry whenever the address bits c1 and c0 change from 11 to 00. The carry output from the first base-4 counter 4CNT1 is applied to an enable terminal of the second base-4 counter 4CNT2 which receives the clock at a clock terminal thereof. Thus, whenever the first base-4 counter 4CNT1 generates the carry, the second base-4 counter 4CNT2 counts the clock to generate the address bits c4 and c3.

Therefore, the interleave read address is generated in combination of the address bits c9, c8, c7, c6, c5 of the third base-18 counter 18CNT3, the address bits c4 and c3 of the second base-4 4CNT2, the address bit c2 of the third binary counter 2CNT3, and the address bits c1 and c0 of the first base-4 counter 4CNT1.

Fig. 5 illustrates a data arrangement when the data is written into the interleave memory at the data rate of 1200bps and 1800bps in accordance with Standard SP-3384 for the CDMA PCS mobile station. Although the addresses in the interleave memory are the same as those in case of 9600bps and 14400bps, the data rate of 1200bps and 1800bps is eight times lower than the data rate of 9600bps and 14400bps. Accordingly, the data to be written into the interleave memory at the data rate of 1200bps and 1800bps are written

at eight sequential addresses. Therefore, the same data appears eight times with respect to the whole data, as shown in Fig. 5. However, the data is interleaved by the address unit during the interleaving.

The data written sequentially into eight addresses are read out according to the interleave read address during the interleaving, and the sequence of the rows of the interleave read addresses is illustrated in Fig. 6. Namely, Fig. 6 illustrates a sequence of the row addresses out of the interleave read addresses. As illustrated, the reading sequence of the rows at the data rate of 1200bps and 1800bps is 1, 9, 2, 10, 3, 11, 4, 12, 5, ..., and 32.

That is, the reading sequence at the data rate of 1200bps and 1800bps is to read 18 columns at the first row and then 18 columns at the ninth row, etc. It is noted that the column sequence is the same as that in case of the data rate of 9600bps and 14400bps, but the row sequence is changed. The row address bits c4, c3, c2, c1 and c0 according to the reading sequence of the rows are represented by 00000, 01000, 00001, 01001, 00010, 01011, ... and 11111.

It is noted from the foregoing descriptions that at the data rate of 1200bps and 1800bps, the bit c3 is first toggled and then toggled in the sequence of the bits c0, c1, c2 and c4. Therefore, the interleave read address generator for the data rate of 1200bps and 1800bps can be realized by changing the output of the interleave read address generator for the data rate of 9600bps and 14400bps. Namely, the output bits c0, c1, c2 and c3 of the interleave read address generator for the data rate of 9600bps and 14400bps are changed respectively to c3, c0, c1 and c2 to realize the interleave read address generator for the data rate of 1200bps and 1800bps.

Fig. 10 illustrates the interleave read address generator for the data rate of 1200bps and 1800bps. The interleave

read address generator generates the interleave read address in the sequence of the interleave read address. The interleave read address generator includes a fourth base-18 counter 18CNT4, fifth and sixth binary counters 2CNT5 and 2CNT6, and a second octal (base-8) counter 8CNT2. The fourth base-18 counter 18CNT4 generates the column address bits c9, c8, c7, c6 and c5 and a carry output in the same manner as the first base-18 counter 18CNT1 shown in Fig. 7, of the interleave read address generator for 9600bps and 14400bps. The carry output from the fourth base-18 counter 18CNT4 is applied to an enable terminal of the fifth binary counter 2CNT5 which receives the clock at a clock terminal thereof. Thus, whenever the fourth base-18 counter 18CNT4 generates the carry output, the fifth binary counter 2CNT5 counts the clock to generate the address bit c3.

The fifth binary counter 2CNT5 generates a carry when the address bit c3 is changed from 1 to 0. The carry output from the fifth binary counter 2CNT5 is applied to an enable terminal of the second octal counter 8CNT2 which receives the clock at a clock terminal thereof. Thus, the second octal counter 8CNT2 counts the clock to generate the address bits c2, c1 and c0, whenever the fifth binary counter 2CNT5 generates the carry.

The second octal counter 8CNT2 generates a carry whenever the address bits c2, c1 and c0 change from 111 to 000. The carry output from the second octal counter 8CNT2 is applied to an enable terminal of the sixth binary counter 2CNT6 which receives the clock at a clock terminal thereof. Thus, whenever the second octal counter 8CNT2 generates the carry, the sixth binary counter 2CNT6 counts the clock to generate the address bit c4.

Therefore, the interleave read address is generated in combination of the address bits c9, c8, c7, c6 and c5 of the fourth base-18 counter 18CNT4, the address bit c4 of the sixth binary counter 2CNT6, the address bit c3 of the fifth binary counter 2CNT5, and the address bits c2, c1 and

c0 of the second octal counter 8CNT2.

As described above, the interleave read address can be freely generated according to the data rates by simply changing the output of the interleave read address generator of 9600bps and 14400bps shown in Fig. 7. Therefore, it is possible to realize the interleave read address generator for every data rates by simply changing the input of the interleave read address generator of 9600bps and 14400bps shown in Fig. 7 according to the data rates.

Fig. 11 illustrates a variable interleave read address generator for generating the interleave read address according to another embodiment of the present invention. As illustrated, the variable interleave read address generator includes a base-18 counter 18CNT5, a base-32 counter 32CNT2 and a multiplexer MUX. The base-18 counter 18CNT5 generates the column address bits c9, c8, c7, c6 and c5 and a carry output in the same manner as the base-18 counter 18CNT1 shown in Fig. 7, of the interleave read address generator for 9600bps and 14400bps. The carry output from the base-18 counter 18CNT5 is applied to an enable terminal of the base-32 counter 32CNT2 which receives the clock at a clock terminal thereof. Thus, whenever the base-18 counter 18CNT5 generates the carry output, the base-32 counter 32CNT2 counts the clock to generate the address bits c4, c3', c2', c1' and c0'.

The multiplexer MUX receives the address bits c3', c2', c1' and c0' from the base-32 counter 32CNT2, to generate the address bits c3, c2, c1 and c0 according to data rate selection signals S3, S2, S1 and S0. Table 3 represents a truth table of the multiplexer MUX.

<Table 3>

Data Rates	S3	S2	S1	S0	c3	c2	c1	c0

9600 & 14400bps	1	0	0	0	c3'	c2'	c1'	c0'
4800 and 7200bps	0	1	0	0	c3'	c2'	c0'	c1'
2400 and 3600bps	0	0	1	0	c3'	c0'	c2'	c1'
1200 and 1800bps	0	0	0	1	c0'	c3'	c2'	c1'

As can be appreciated from Table 1, the multiplexer MUX generates different address bits c3, c2, c1 and c0 according to the data rate selection signals S3, S2, S1 and S0. For example, in case of the data rate of 9600bps and 14400bps, the multiplexer MUX generates the data bits c3', c2', c1' and c0' at the output terminals c3, c2, c1 and c0, respectively. At that moment, the interleave read address generator has the same function as the interleave read address generator of Fig. 7. The interleave read address for 9600bps and 14400bps is generated in combination of the address bits c9, c8, c7, c6 and c5 of the base-18 counter 18CNT5, the address bit c4 of the base-32 counter 32CNT2, and the address bits c3, c2, c1 and c0 of the multiplexer MUX.

Further, in case of the data rate of 4800bps and 7200bps, the multiplexer MUX generates the data bits c3', c2', c0' and c1' at the output terminals c3, c2, c1 and c0, respectively. At that moment, the interleave read address generator has the same function as the interleave read address generator of Fig. 8. The interleave read address for 4800bps and 7200bps is generated in combination of the address bits c9, c8, c7, c6 and c5 of the base-18 counter 18CNT5, the address bit c4 of the base-32 counter 32CNT2, and the address bits c3, c2, c1 and c0 of the multiplexer MUX.

In case of the data rate of 2400bps and 3600bps, the multiplexer MUX generates the data bits c3', c0', c2' and c1' at the output terminals c3, c2, c1 and c0,

respectively. At that moment, the interleave read address generator has the same function as the interleave read address generator of Fig. 9. The interleave read address for 2400bps and 3600bps is generated in combination of the address bits c9, c8, c7, c6 and c5 of the base-18 counter 18CNT5, the address bit c4 of the base-32 counter 32CNT2, and the address bits c3, c2, c1 and c0 of the multiplexer MUX.

Moreover, in case of the data rate of 1200bps and 1800bps, the multiplexer MUX generates the data bits c0', c3', c2' and c1' at the output terminals c3, c2, c1 and c0, respectively. At that moment, the interleave read address generator has the same function as the interleave read address generator of Fig. 10. The interleave read address for 1200bps and 1800bps is generated in combination of the address bits c9, c8, c7, c6 and c5 of the base-18 counter 18CNT5, the address bit c4 of the base-32 counter 32CNT2, and the address bits c3, c2, c1 and c0 of the multiplexer MUX.

In the meantime, the multiplexer MUX is composed of first through sixteenth AND gates AND1-AND16 and first through fourth OR gates OR1-OR4. The address bit c0' from the base-32 counter 32CNT2 is applied to the fourth, seventh, tenth and thirteenth AND gates AND4, AND7, AND10 and AND13. The address bit c1' from the base-32 counter 32CNT2 is applied to the first, fifth, ninth and fourteenth AND gates AND1, AND5, AND9 and AND14. The address bit c2' from the base-32 counter 32CNT2 is applied to the second, sixth, eleventh and fifteenth AND gates AND2, AND6, AND11 and AND15. Besides, the address bit c3' from the base-32 counter 32CNT2 is applied to the third, eighth, twelfth and sixteenth AND gates AND3, AND8, AND12 and AND16.

The data rate selection signal S3 is commonly applied to the first through fourth AND gates AND1-AND4. Thus, a set of the first through fourth AND gates AND1-AND4 generates the address bits c0', c3', c2' and c1' at the output

terminals c3, c2, c1 and c0 respectively in response to the data rate selection signal S3 of the logic high level, so as to generate the interleave read address for 1200bps and 1800bps.

Similarly, the data rate selection signal S2 is commonly applied to the fifth through eighth AND gates AND5-AND8. Thus, a set of the fifth through eighth AND gates AND5-AND8 generates the address bits c3', c0', c2' and c1' at the output terminals c3, c2, c1 and c0 respectively in response to the data rate selection signal S2 of the logic high level, so as to generate the interleave read address for 2400bps and 3600bps.

The data rate selection signal S1 is commonly applied to the ninth through twelfth AND gates AND9-AND12. Thus, a set of the ninth through twelfth AND gates AND9-AND12 generates the address bits c3', c2', c0' and c1' at the output terminals c3, c2, c1 and c0 respectively in response to the data rate selection signal S1 of the logic high level, so as to generate the interleave read address for 4800bps and 7200bps.

Further, the data rate selection signal S0 is commonly applied to the thirteenth through sixteenth AND gates AND13-AND16. Thus, a set of the thirteenth through sixteenth AND gates AND13-AND16 generates the address bits c3', c2', c1' and c0' at the output terminals c3, c2, c1 and c0 respectively in response to the data rate selection signal S1 of the logic high level, so as to generate the interleave read address for 9600bps and 14400bps.

The first OR gate OR1 receives the outputs from the first, fifth, ninth and thirteenth AND gates AND1, AND5, AND9 and AND13 to generate the address bit c3. The second OR gate OR2 receives the outputs from the second, sixth, tenth and fourteenth AND gates AND2, AND6, AND10 and AND14 to generate the address bit c2. The third OR gate OR3 receives the outputs from the third, seventh, eleventh and fifteenth

AND gates AND3, AND7, AND11 and AND15 to generate the address bit c1. The fourth OR gate OR4 receives the outputs from the fourth, eighth, twelfth and sixteenth AND gates AND4, AND8, AND12 and AND16 to generate the address bit c0.

As described in the foregoing, the interleave read address generator of the invention is realized by inexpensive counters. Further, a variable interleave read address generator of the invention includes a multiplexer to generate the variable interleave read address for various data rates. Therefore, it is possible to provide the interleave read address generator at low cost.

CLAIMS

1. An interleaver for use in a CDMA mobile station comprising:

an interleave memory arranged into a matrix of 2^n rows and m columns (where m and n are integers);

means for writing interleave data to the interleave memory in column order and, within each column, in row order;

an interleave read address generator comprising a base-m counter for counting a clock input modulo-m, to generate a column address, and a base-2^n counter for counting carry outputs from the base-m counter modulo-2^n, to generate a row address; and

means for reading the interleave data from the interleave memory at the position corresponding to the column and row addresses from the interleave read address generator.

2. An interleaver according to claim 1 in which m is 18 and n is 5.

3. An interleaver according to claim 1 or claim 2 for a data rate of 9600bps or 14400bps, in which the column address is equal to the current value of the base-m counter and the row address is equal to the current value of the base-2^n counter.

4. An interleaver according to claim 1 or claim 2 for a data rate of 4800bps or 7200bps, in which the column address is equal to the current value of the base-m counter and the row address is equal to the current value of the base-2^n counter with the positions of the two least significant bits (LSB and LSB+1) being altered as follows:

LSB -> LSB+1;
LSB+1 -> LSB.

5. An interleaver according to claim 1 or claim 2 for a data rate of 2400bps or 3600bps, in which the column

address is equal to the current value of the base-m counter and the row address is equal to the current value of the base-2^n counter with the positions of the three least significant bits (LSB, LSB+1 and LSB+2) being altered as follows:

LSB	->	LSB+2;
LSB+2	->	LSB+1;
LSB+1	->	LBS.

6. An interleaver according to claim 1 or claim 2 for a data rate of 1200bps or 1800bps, in which the column address is equal to the current value of the base-m counter and the row address is equal to the current value of the base-2^n counter with the positions of the four least significant bits (LSB, LSB+1, LSB+2 and LSB+3) being altered as follows:

LSB	->	LSB+3;
LSB+3	->	LSB+2;
LSB+2	->	LSB+1;
LSB+1	->	LSB.

7. An interleaver for use in a CDMA mobile station comprising:

an interleave memory arranged into a matrix of 2^n rows and m columns (where m and n are integers);

means for writing interleave data to the interleave memory in column order and, within each column, in row order;

an interleave read address generator comprising a base-m counter for counting a clock input modulo-m, to generate a column address, and a base-2^n counter for counting carry outputs from the base-m counter modulo-2^n, to generate a row count value and a multiplexer for changing the positions of the bits of the row count value according to one or more data rate selection signals, to generate a row address; and

means for reading the interleave data from the interleave memory at the position corresponding to the column and row addresses from the interleave read address

generator.

8. An interleaver according to claim 7 in which m is 18 and n is 5.

9. An interleaver according to claim 7 or claim 8 for a data rate of 9600bps or 14400bps, in which the multiplexer outputs the bits of the row count value unchanged in response to a first data rate selection signal.

10. An interleaver according to any one of claims 7-9 for a data rate of 4800bps or 7200bps, in which the multiplexer changes the positions of the two least significant bits (LSB and LSB+1) of the row count value as follows in response to a second data rate selection signal:

LSB -> LSB+1;
LSB+1 -> LSB.

11. An interleaver according to any one of claims 7-10 for a data rate of 2400bps or 3600bps, in which the multiplexer changes the positions of the three least significant bits (LSB, LSB+1 and LSB+2) of the row count value as follows in response to a third data rate selection signal:

LSB -> LSB+2;
LSB+2 -> LSB+1
LSB+1 -> LSB.

12. An interleaver according to any one of claims 7-11 for a data rate of 1200bps or 1800bps, in which the multiplexer changes the positions of the four least significant bits (LSB, LSB+1, LSB+2 and LSB+3) of the row count value as follows in response to a fourth data rate selection signal:

LSB -> LSB+3;
LSB+3 -> LSB+2
LSB+2 -> LSB+1
LSB+1 -> LSB.

13. An interleaver for use in a CDMA mobile station, the interleaver being substantially as described with reference

to any one of FIGs. 7-11 of the accompanying drawings.

The Patent Office

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Application No: GB 9720859.9 **Examiner:** Ken Long
Claims searched: 1 to 13 **Date of search:** 10 December 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4P (PEL)

Int Cl (Ed.6): H03M 13/22

Other: ONLINE : WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB 2294616 A	Nokia (page 3 lines 25 to 33 and page 20 line 1 to page 21 line 7)	1
Y	GB 2191914 A	Thorn EMI Ferguson (page 3 line 36 to page 4 line 49 and page 2 lines 23 to 35)	1
A	EP 0608079 A2	Matsushita (column 6 line 48 to column 7 line 13 and column 7 lines 40 to 49)	1
A	WO 95/30956 A1	Motorola (page 14 line 10 to page 15 line 4)	1
A	WO 95/16310 A1	Nokia (page 1 lines 1 to 8 and page 6 lines 12 to 21)	1
Y	US 5136588	Kabushiki Kaisha CSK (column 1 lines 31-45, column 2 lines 1-4 & 31-38 and column 4 lines 40-60)	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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(54) Interleave read address generator

(57) An interleaver for use in a CDMA mobile station is arranged into a matrix of 32 rows and 18 columns. Interleave data is written to the interleave memory in column order and, within each column, in row order. A base-18 counter counts a clock input modulo-18, to generate a column address c5-c9, and a base-32 counter counts carry outputs from the base-18 counter modulo-32, to generate a row count value. A multiplexer MUX changes the positions of the bits of the row count value according to one or more data rate selection signals S0-S3, to generate a row address c0-c4. The interleave data is read from the interleave memory at the position corresponding to the column and row addresses.

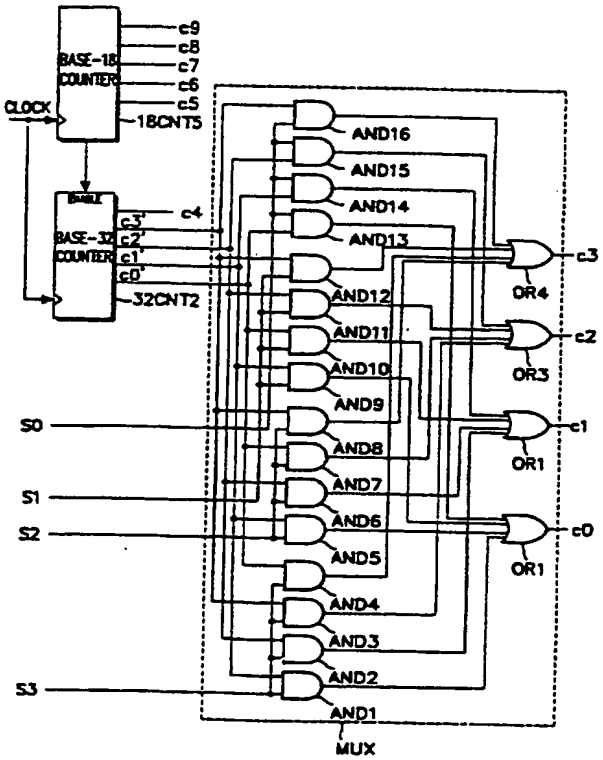

FIG. 11